Thin film transistor modeling: Frequency dispersion

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Thin film transistor modeling: frequency dispersion

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Outline

• Motivation
• Compact model challenges
• Effective medium approach
• Current-voltage characteristics
  – UCCM
  – Advanced (non-ideal and contact effects)
• Capacitance-voltage characteristics and Dispersion
• Sensing applications
• Noise
• Conclusions
Cost of x-Si transistors going up

- 2002: 180 nm
- 2004: 130 nm
- 2006: 90 nm
- 2008: 65 nm
- 2010: 40 nm
- 2012: 28 nm
- 2014: 20 nm
- 2015: 16 nm

4 companies left:
- Samsung
- TSMC
- Global Foundry
- Intel

22 companies compete
($2B cost of entry)

4 companies left
($7B cost of entry)
Ballistic mobility in Si


TFT Field Effect Mobility

The diagram shows the relationship between mobility (cm^2/Vs) and processing temperature (°C) for different types of TFTs:

- **x-Si**
- **Oxide TFTs**
- **poly-Si TFTs**
- **a-Si TFTs**

Organic TFTs are represented by a yellow area.
FETs and TFTs

X-Si

From http://www.tradekorea.com/product/detail/P293787/TFT-LCD-Glass-Slimming.html
See-through $1 smart phone

From https://futurephones2000.wordpress.com/
TFTs could be on flexible substrates for robotics applications
Challenges to TFT Compact Modeling from Applications

- Higher resolution, interactive displays
- Higher speed for RFIDs and sensors
- Low temperature processing for flexible electronics, and computers on glass

Pushing TFT designs to the limits with less ideal characteristics – challenge for compact modeling

TFT Modeling: Challenges

• Different device sections (intrinsic channel versus contacts) dominate depending on bias and/or temperature
• Parameter variations from device to device
• Non trivial scaling
• Dispersion
• Noise
Effective medium approach and Unified Charge Control Model (UCCM)
TFT layout and circuit elements

High gate bias – Contact Control

- Source
- Channel α-Si
- Gate Dielectric
- Gate

n+

Drain

Low gate bias – Channel Control
TFT layout and circuit elements

High gate bias – Contact Control

Source

n+

Gate Dielectric

Channel $\alpha$-Si

Gate

Drain

Low gate bias – Channel Control
TFT layout and circuit elements

High gate bias – Contact Control

- Source
- Drain
- Channel α-Si
- Gate Dielectric
- Gate

n+

Low gate bias – Channel Control
TFT layout and circuit elements

High gate bias – Contact Control

Gate Dielectric

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Source

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n+
TFT layout and circuit elements

High gate bias – Contact Control

Source

n+

Drain

Channel α-Si

Gate

Low gate bias – Channel Control

Gate Dielectric

Source
TFT layout and circuit elements

High bias – Contact Control

Source

n+

Drain

Gate

Gate Dielectric

α-Si

Channel

Low bias – Channel Control

D3

R

D4

D1

R1

D2

Vg

mn2

mn

mn1

Vdd

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TFT Modeling: Goals

Great lawyers will find a way to turn the tables in your favor

Good modelers
Deep and tail localized states

\[ g(E) = g_d \exp\left(\frac{E - E_C}{kT_d}\right) + g_t \exp\left(\frac{E - E_C}{kT_t}\right) \]

Deep and tail localized states

\[ g(E) = g_d \exp\left( \frac{E - E_C}{kT_d} \right) + g_t \exp\left( \frac{E - E_C}{kT_t} \right) \]

Deep and tail localized states

\[ g(E) = g_d \exp\left(\frac{E - E_C}{kT_d}\right) + g_t \exp\left(\frac{E - E_C}{kT_t}\right) \]

Field Effect Mobility vs, Gate Voltage Swing

\[ \mu_{FET} = \mu \frac{n_s}{n_{TOTAL}} \]
The field effect mobility is the effective mobility that links channel transport to the MOS capacitor properties:

\[
\frac{\mu_{f_{\text{et}}}}{\mu_0} = \frac{N_{\text{free}}}{N_{\text{free}} + N_{\text{loc}}}
\]

\[
\frac{1}{\mu_{f_{\text{et}}}} = \frac{1}{\mu_0} + \frac{1}{\mu_1 \cdot \left( \frac{2qV_{g_{\text{te}}}}{\eta_f kT} \right)^{m\mu}}
\]

\[
V_{g_{\text{te}}} = \eta \frac{kT}{q} \left( 1 + \frac{\alpha_{\text{sat}} qV_{g_{\text{t}}}}{2\eta kT} + \sqrt{\Delta^2 + \left[ \frac{\alpha_{\text{sat}} qV_{g_{\text{t}}}}{2\eta kT} \right]^2} \right)
\]

RPI TFT model

Unified Charge Control Model

\[ V_{GS} - V_T = q \left( \frac{n_s - n_o}{c_a} \right) + V_{sub} \ln \left( \frac{n_s}{n_o} \right) \]

\[ V_{sub} = \eta \frac{k_B T}{q} \]

ABOVE THRESHOLD
Unified Charge Control Model

\[ V_{GS} - V_T = q \left( n_s - n_o \right) / c_a + V_{sub} \ln \left( \frac{n_s}{n_o} \right) \]

\[ V_{sub} = \eta \frac{k_B T}{q} \]

Below threshold

\[ (V - V_T) / V_{sub} \] vs \[ (V - V_T) / V_{sub} \]
Unified Charge Control Model

\[ V_{GS} - V_T = q \left( \frac{n_s - n_o}{c_a} \right) + V_{sub} \ln \left( \frac{n_s}{n_o} \right) \]

\[ V_{sub} = \eta \frac{k_B T}{q} \left( \frac{n_s}{n_o} \right) \]

Graphs showing the relationship between \( V_{GS} - V_T \) vs. \( (V-V_T)/V_{sub} \) and \( (V-V_T)/V_{sub} \) vs. \( n_s/n_o \).
**UCCM saturation current for different TFTs**

![Graph showing saturation current for different materials: x-Si, CNT, Pentacene, ZnO, mX-Si, a-Si. The x-axis represents gate voltage (V), and the y-axis represents saturation current (A/m).](image)

\[ I_{sat} = \frac{g_{ch} V_{gte}}{1 + g_{ch} R_s + \sqrt{1 + 2 g_{ch} R_s + \left(\frac{V_{gte}}{V_L}\right)^2}} \]

\[ V_{gte} = V_{sub} \left[ 1 + \frac{V_{GT}}{2V_{sub}} + \sqrt{\delta^2 + \left(\frac{V_{GT}}{2V_{sub}} - 1\right)^2} \right] \]

\[ I_{ds} = \frac{g_{ch} V_{ds}}{\left[1 + \left(\frac{g_{ch} V_{ds}}{I_{sat}}\right)^m\right]^{1/m}} \]
Simulated I-Vs. $L = 10 \, \mu m$

- Left graph: $L_{\text{CHANNEL}} = 10 \, \mu m$, $V_D = 0.1 \, V$
  - Measurement
  - AimSpice model

- Right graph: $L_{\text{CHANNEL}} = 10 \, \mu m$, $V_D = 10.1 \, V$
  - Measurement
  - AimSpice model
UTMOST-IV Delivers Full Capability of RPI TFT Models

Introduction
Simucad SmartSpice has been a de facto standard analog circuit simulator from the inception of the TFT (Thin Film Transistor) technology industry. The early introduction of SPICE compact models developed by Rensselaer Polytechnic Institute (RPI) for poly silicon (poly-Si) and amorphous silicon (a-Si) TFT devices made integrated circuit design possible. Simucad UTMOST-III SPICE parameter extraction tool played a critical role by providing the TFT model parameters for circuit designers. Modeling engineers have accumulated complicated non-linear equations would fail to reveal the potential capability unless good initial parameter values are obtained.

UTMOST-IV Hybrid Optimizer: A Combination of Two Optimization Algorithms
UTMOST-IV provides six optimization algorithms. Two out of six are called as the local optimization algorithm, and the rest are the global optimization algorithm. The local optimizers require reasonable initial parameter values, while the global optimizers do not. Application
Non-ideal behavior (2D generation model)

Effective gate length and width for scaling design

\[ L_{\text{eff}} = L - \Delta L(V_G, V_D) \]

\[ W_{\text{eff}} = W + \Delta W(V_G, V_D) \]
Graphene and MoS$_2$ FET I-Vs

Sensing Applications

Gas Gated Transistor

> 220 °C


Selective Sensing with One Device

Equivalent Circuit: add leakage

Channel transistor

Contact transistor

Diode

Leakage

Added leakage path
TFT Transfer Characteristics: large, drain bias dependent leakage

Threshold Voltage dependence on geometry for scaling

\[ V_{TH} = V_{thx} - \frac{at \cdot V_{ds}^2 + bt}{(V_{ds} - (V_{thx} - \text{vsigmat})) \cdot \left(1 + \frac{1}{\text{vsigma}}\right)} \]
Improved effective TFT mobility model

\[ m_{\text{eff}} = \mu_s + \frac{m_{\text{fet}}}{1 + \frac{\theta}{\tau_o x} \cdot V_{\text{gte}}} \]

\[ \frac{1}{m_{\text{fet}}} = \frac{1}{\mu_0} + \frac{1}{\mu_1 \cdot \left( \frac{2 \cdot V_{\text{gte}}}{\eta f \cdot V_t} \right)^{mmu}} \]

where

\[ V_t = k \cdot T/q \]

\[ V_{\text{gte}} = \eta \cdot V_t \cdot \left( 1 + \frac{\alpha_{\text{sat}} \cdot V_{\text{gt}}}{2 \cdot \eta \cdot V_t} + \sqrt{\delta^2 + \left( \frac{\alpha_{\text{sat}} \cdot V_{\text{gt}}}{2 \cdot \eta \cdot V_t} - 1 \right)^2} \right) \]

\[ V_{\text{gt}} = V_{\text{gs}} - V_{\text{th}} \]
Unified Electron Sheet Charge Density Per Unit Area (2D generation model)

\[ V_{ds} = \frac{V_{ds}}{1 + \left( \frac{V_{ds}}{V_{dsat}} \right)^{mss} 1/mss} \]

\[ n_s = 2 \cdot n_0 \cdot \log \left( 1 + \frac{1}{2} \cdot e^{\frac{V_{gs}}{eta_f \cdot V_t}} \right) \quad \text{eta}_f = \frac{eta}{1 + meta \cdot reta \cdot \frac{i1}{1 + i1}} \]

\[ n_0 = \frac{\varepsilon_{SiO_2} \cdot eta \cdot V_t}{2 \cdot q \cdot tox} \]
Scaling with RPI TFT model

Reciprocal channel current, $1/A$

Channel Length, $\mu$m

- VD = 0.1 V
- Model fit
Scaling with RPI TFT model

Reciprocal channel current, \( \frac{1}{A} \)

Channel Length, \( \text{um} \)

VD = 10.1 V

Model fit

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CONTACT EFFECTS
The effect of contact non-linearity (diode). More pronounced for shorter channels.
Contact Nonlinearity Affects Short Channel Devices

- **3.5 micron**
  - $V_t = 1.4\ V$
  - $V_g = 10\ V$
  - $V_g = 20\ V$

- **10 micron**
  - $V_t = 2\ V$
  - $V_g = 5\ V$
  - $V_g = 10\ V$
  - $V_g = 15\ V$
  - $V_g = 20\ V$

- **300 micron**
  - $V_t = 4\ V$
  - $V_g = 15\ V$
  - $V_g = 20\ V$
The effect of contact non-linearity is closely related to the threshold voltage variation. The contact section must be modeled separately.
Contact transistor model

Contact transistor

Channel transistor

V1

V2

Diode

Leakage

Vds
Node voltages. Solid - channel potential on the source side, dashed - on the drain side. $L = 1 \ \mu m$

At large gate bias, the voltage drop across the intrinsic transistor is small.

$V_D =$
- 0.1 V
- 5.1 V
- 10.1 V

$L_{S-D} = 1 \ \mu m$

Voltage drop across channel

Channel transistor

Drain potential

Contact transistor

Drain potential

Node voltage ratio

Gate Bias, V
Node voltages. Solid - channel potential on the source side, dashed - on the drain side. $L = 10 \, \mu m$

$L_{S-D} = 10 \, \mu m$

- Voltage drop across channel
- Channel transistor
- Drain potential
- Contact transistor
- Drain potential
- Node voltage ratio
- Gate Bias, $V_D$

$V_D =$
- 0.1 V
- 5.1 V
- 10.1 V

Contact transistor
Diode
Leakage

$V_{ds}$
The channel of the transistor should be modeled as a distributed RC line with gate controlled resistances. Additional contact associated capacitances have significant dependence on the gate bias and should also be modeled as transistor capacitances.
Capacitance model:
Intrinsic and parasitic capacitances
Capacitance Dispersion

![Graph showing capacitance dispersion with various frequency labels and capacitance values plotted against frequency.

- w100L20Fr1000HzLOut
- w100L20Fr2000HzLOut
- w100L20Fr5000HzLOut
- w100L20Fr10000HzLOut
- w100L20Fr20000HzLOut
- w100L20Fr50000HzLOut
- w100L20Fr100000HzLOut
- w100L20Fr500HzLout
- w100L20Fr700HzLout]
Capacitance Model: Equations

When capmod=0,

\[ C_{gs} = C_f + \frac{2}{3} \cdot C_{gcs} \cdot \left[ 1 - \left( \frac{V_{dsat} - V_{dse}}{2 \cdot V_{dsat} - V_{dse}} \right)^2 \right] \]

\[ C_{gd} = C_f + \frac{2}{3} \cdot C_{gcd} \cdot \left[ 1 - \left( \frac{V_{dsat}}{2 \cdot V_{dsat} - V_{dse}} \right)^2 \right] \]

\[ C_f = \frac{1}{2} \cdot \varepsilon_{si} \cdot w \]

\[ C_{ges} = \frac{w \cdot l \cdot \varepsilon_{SiO_2}/t_{ox} \cdot \left( \frac{V_{g}}{\varepsilon_{red} \cdot V_t} \right)}{1 + \eta_{cd} \cdot \varepsilon} \]

\[ C_{gcd} = \frac{w \cdot l \cdot \varepsilon_{SiO_2}/t_{ox} \cdot \left( \frac{V_{g} - V_{dse}}{\eta_{cd} \cdot V_t} \right)}{1 + \eta_{cd} \cdot \varepsilon} \]

\[ \eta_{cd} = \varepsilon_{red} + \varepsilon_{red0} \cdot V_{dse} \]
**Capacitance data**

For 5 micron overlap $C_c = 0.125$ PF
For 3.5 micron gate $C_t = 0.34$ pF

$C_t = C_{ch} + a L_{overlap} + C_o$

Gate oxide (ON state) capacitance scaling. The offset corresponds to contact capacitance
Frequency dispersion

The device channel was divided into 20 sub-regions in order to account for the distributed channel resistance. Good agreement with the experiment is obtained. The experimental threshold shift with frequency is trap-related.
Physics of capacitance Dispersion: Transit Time Mechanism

At low frequencies, electrons have time to travel to the middle of the channel establishing the second plate of for the parallel plate channel capacitance.

At high frequencies, electrons DO NOT have time to travel to the middle of the channel and the capacitance is smaller.

Since the field (and velocity driving electrons is proportional to $1/L$, this dispersion is proportional to $1/L^2$.

$$\tau_1 = \frac{L_g^2}{\mu_{FET} \cdot V_{eff}}$$
Elmore model
Complete circuit

Transmission line model
2D model
Traps lead to a strong dispersion in C-V characteristics

Role of traps

- Traps and contacts determine TFT I-V and C-V characteristics
- Traps cause noise and their density can be extracted from noise
- Frequency dispersion is determined by localized traps
  - The rate of traps interaction with the states above mobility edge
  - The trap-dominated speed of electron propagation along the channel
- Contacts are non-linear and dominant at higher currents and shorter channel lengths
Variable dispersion model

\[ V_{th\_effective} = \frac{kT_{effective}}{q} = \frac{kT}{q} \left(1 + \frac{f}{f_e}\right)^{mf} \]

\[ f_e = \frac{1}{\tau_e} \]

At low densities in the channel, traps take a longer time to exchange with extended states than the transit time.

Application of dispersion for light sensing

Implementation

Light sensor

Equivalent parallel capacitance; $C_p \text{ (F)}$

Irradiance (arb. units)

Wavelength (nm)

- 465 nm
- 525 nm
- 636 nm

Traps lead to TFT characteristics dependence on ambient light

Non-linear dependence on illuminance

NOISE
Gate voltage dependent 1/f noise

Noise much large in short channel devices

Trap density can be extracted from noise data

Noise: TFTs and Crystalline FETs (after [1])

References

CONCLUSIONS

• The challenge in the compact modeling of Thin Film Transistors (TFTs) is to accurately reproduce all regimes of operation (leakage, subthreshold, and above threshold)

• The developed models are suitable for the device characterization and parameter extraction even for the TFTs with non-ideal behavior

• These models account for non-ideal effects including gate-dependent mobility, contact effects and capacitance dispersion
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