TERAHERTZ TESTING OF VERY LARGE SCALE INTEGRATED CIRCUITS

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Growing sophistication of electronics devices and circuits and, especially of VLSI and ULSIC, presents
increasing demands on circuit testing and fault diagnosis. The conventional well-established technique
of electric AC and DC testing is costly, does not assure a complete fault identification. This technique also
presents an additional security problem making it possible to design faked circuits avoiding the identification by
this testing. Fabrication of and even perception of faked VLSI capable of surreptitious performance has become
an increasing problem often referred to as “trojan hardware”. Experimental techniques, such as laser
scanning and terahertz imaging have a limited resolution signal-to-noise ratios and encounter difficulties in
defect identification. A new approach of THz testing of Microwave Monolithic Integrated Circuits (MMICs), VLSI,
and ULSIC is based on measuring the circuit responses at the pins or input/output leads and comparing these
responses with etalon responses. This technique could augment or replace the electrical testing and/or laser
and THz scanning testing for production testing, burn-in testing, high temperature testing, and infant mortality
testing. It could also be extended for the fault diagnosis and identification and for the lifetime and reliability
predictions. To this end it could be augmented by the low noise measurements. The number of the detected
responses could be very large, since the permutations of the voltages between the pins and leads could be
measured at the different positions of the scanning THz beam, different THz frequencies and polarizations, in
the pulsed and/or CW mode, at the different modulation frequencies and at the different THz intensities. This
technique could be used under or without bias. The processing of these responses forming multi-dimensional
images in the excitation parameter space could be processed using artificial intelligence algorithms and
machine learning approaches making this testing technique self-learning and self-improving. This testing could
be further improved by designing for testability by THz responses at the pins.

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References
Circuits and systems conference, DOI: 10.1109/NEWCAS.2011.5981325
time-frequency scan of VLSI. Microelectronics Reliability, 64, 299–305. doi:10.1016/j.microrel.2016.07.052
integrated circuits using enhanced-spatial-resolution terahertz time-domain spectroscopy and imaging,” Optics
and Lasers in Engineering, vol. 104, pp. 274–284, 2018
4. M. Nagel and H. Kurz, Terahertz imaging: Terahertz reflectometry images faults in silicon chips, Laser Focus
World, 11/01/2011
pp. 5487-5490 (2017)
7. G. Rupper, J. Suarez, S. Rudin, M. Reed, M. Shur, Terahertz plasmonics for testing very large-scale
2018
8. M. Shur, S. Rudin, G. Rupper, M. Reed, and J. Suarez, Sub-Terahertz Testing of Millimeter Wave Monolithic
and Very Large Scale Integrated Circuits, Solid State Electronics (2019), to be published