LOW-TEMPERATURE PROCESSED InGaZnO MES-FET FOR FLEXIBLE DEVICE APPLICATIONS

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Amorphous oxide semiconductor (AOSs) of an In-Ga-Zn-O (IGZO)[1)] is expected to be used as a channel material for thin-film transistors (TFTs) because the IGZO TFTs exhibit field-effect motility (μ_{FE}) of over 10 cm^2/Vs and good uniformity even fabricate at room temperature. The oxide TFTs with metal-insulator-semiconductor (MIS) structure have been employed widely; however, maximum processing temperature of 300-400 °C is required to guarantee the performance and reliability of the TFTs. In contrast, metal-semiconductor field effect transistor (MES-FET) has several advantages especially for flexible devices since a Schottky gate can be formed at low temperature with AOSs. There are a few reports of AOSs based MES-FET[2, 3)]; however, it has remained an issue to form stable and good Schottky contact on the AOSs. We reported the top-gated MES-FET with the IGZO channel, which was deposited by mist chemical vapour deposition at 350 °C, and sputtered silver oxide (AgOx) Schottky gate[4)]. The μ_{FE} of 3.2 cm^2/Vs and subthreshold swing (SS) of 356 mV/decade were achieved. However, a maximum processing temperature of the MES-FET was 350 °C, which was not suitable for flexible device applications.

In this presentation, the IGZO MES-FET with AgOx Schottky gate was fabricated at a maximum processing temperature of 150 °C. We investigated the influences of deposition conditions and post-deposition annealing on electrical properties of the low-temperature processed IGZO MES-FET.

Figure 1 shows a cross sectional view of the IGZO MES-FET. First, a 100 nm-thick IGZO film was deposited on glass substrate by DC magnetron sputtering without intentional substrate heating from InGaZnO (In:Ga:Zn=1:1:1 mol.%) target. Deposition pressure was kept at 1.0 Pa, while the O_2 gas ratio [$R(O_2)=O_2/(Ar+O_2)$] was varied at 0.66, 0.80, and 1.00%. The IGZO film was patterned into an active channel by conventional photolithography and wet etching. The IGZO channel was then annealed at 100 or 150 ºC for 1h in ambient air. A 120 nm-thick AgOx was deposited by DC reactive sputtering, and Au was deposited on the AgOx by thermal evaporation. The AgOx/Au stacked Schottky gate was patterned by lift-off. Finally, Mo source and drain electrodes was formed by lift-off. Channel width/length of the MES-FET was 100/10 µm.

Figure 2 shows the (a) forward and reverse currents of the IGZO/AgOx Schottky diode and (b) on and off current of the IGZO MES-FET, as a function of the Hall carrier concentration (N_{Hall}) in the IGZO channel. The diode properties were well correlated with the N_{Hall}; however, on-current of the MES-FET depended on not only N_{Hall} but also the R[O_2] of the IGZO deposition.

Carrier transport mechanism of the IGZO MES-FET and control methods of electrical properties will be discussed at the conference.

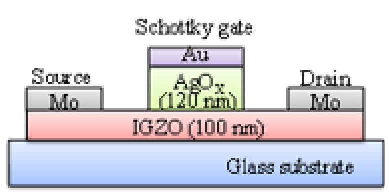

Fig. 1 Cross sectional view of the IGZO MES-FET.

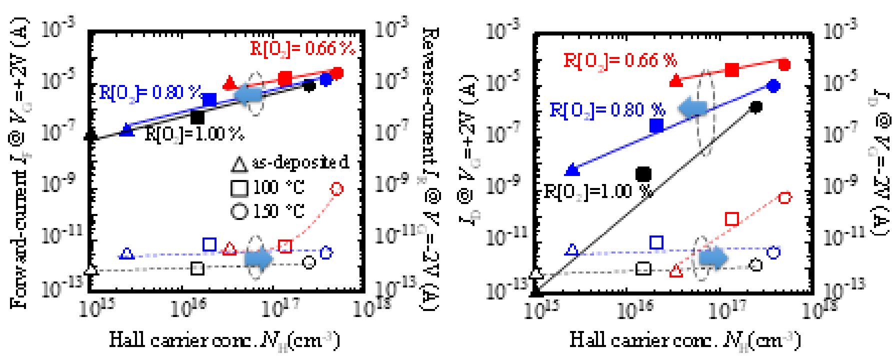

Fig. 2 (a) Forward and reverse currents of Schottky diode and (b) on and off current of the IGZO MES-FET, as a function of N_{Hall} in IGZO channel.

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