

TFT AND ULSI TECHNOLOGIES; THE PARALLEL EVOLUTION OF THE RESEARCH AND THE HIGHER EDUCATION IN FRANCE

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This paper deals with the evolution since the early eighties of the microelectronics applied to integrated circuits and to large area electronics. The evolution in France was linked to a very strong effort of the French government (Microelectronics national plan) to improve the Higher Education in this field and to form with the knowledge and the know-how the future engineers, masters and doctors to the research and development and to the production. A way to help the growth of microelectronics companies mainly in France, but also for the world in the frame of multinational companies. More recently, a new national plan was engaged in the frame of the French Large Investment Commissariat with the goal to improve the large area technology and the integrated technologies and to be adapted to the digital society coming. Connecting objects and Internet of Things are mainly mixing the different components of the electronics and microelectronics domains [1]. After a synthetic presentation of the evolution of the two main technologies developed in research and development centers and in academic laboratories, the paper highlights the strategy developed by the French community based on the innovation [2]. The interesting point is that, if at the beginning the two domains appear independent, the evolution of the process and the fabulous evolution of the CAD tools is making closer and closer the design and fabrication approaches by combining the two technologies. For example the FDSOI (Fully Depleted Silicon on Insulator) concept was in practice existing since many years in thin film transistor technology deposited at a relatively low temperature ($<600^{\circ}\text{C}$) [3]. The arrival on the market of the first systems-on-chip (SOC) and systems-in-package (SIP) with a wide spectrum of applications [4] confirms this interpenetration which has also a multidisciplinary aspect [5]. The new technologic process developed by French LETI laboratory, entitled CoolcubTM, combines the classical VLSI technology with thin film technology in a three dimensional stacking at a relatively low temperature [6]. This evolution induces a huge change in the pedagogical approach in order to maintain a good background, skills and know-how for the research, development and fabrication activities [7-8]. The end of the paper will be devoted to the presentation of several examples of innovative projects, proposed to the students that must have this double competence of the thin film electronics and of the ultra-large scale-integration microelectronics moving to nanoelectronics. A way to prepare the evolution of this field that is the heart of most objects of the near future.

References

- [1] M. Swaminathan, J.M. Pettit, 3rd System Integration Workshop (2011)
- [2] O. Bonnaud and L. Fesquet, Innovation in Higher Education: specificity of the microelectronics field, Oral presentation, Proc. of IEEE SBMicro'2016, Belo Horizonte (MG - Brasil), 1-5 Sept. DOI: 10.1109/SBMicro.2016.7731342, Pp: 1-4, 2016
- [3] L. Pichon, F. Raoult, O. Bonnaud, H. Sehil, D. Briand, Conduction behaviour of low temperature ($\leq 600^{\circ}\text{C}$) Polysilicon TFT with an in-situ drain doping level, Solid State Electronics, Vol 38, n°8 (1995) pp 1515-1521
- [4] O. Bonnaud, New Approach for Sensors and Connecting Objects Involving Microelectronic Multidisciplinarity for a Wide Spectrum of Applications, International Journal of Plasma Environmental Science & Technology, vol. 10, no. 2, pp. 115-120, 2016
- [5] O. Bonnaud, The Multidisciplinary Approach: a Common Trend for ULSI and Thin Film Technology, ECS Transaction, 05/2015; 67(1):147-158. DOI:10.1149/06701.0147ecst
- [6] Batude, P., et al., "Demonstration of low temperature 3D sequential FDSOI integration down to 50nm gate length," 2011 Symposium on VLSI Technology Digest of Technical Papers, pp. 158-159.
- [7] O. Bonnaud and L. Fesquet, Innovating projects as a pedagogical strategy for the French network for education in microelectronics and nanotechnologies, Proc. of IEEE Int. Conf. on Microelectronic Systems Education (MSE'13), Print ISBN: 978-1-4799-0139-5, pp. 5-8, 2013
- [8] O. Bonnaud, L. Fesquet, Towards multidisciplinary for microelectronics education: a strategy of the French national network, MSE'2015, Pittsburg-PA-USA, May 2015, Proc.: 978-1-4799-9915-6/15/\$31.00 ©2015 IEEE, Pp: 1-4 (2015)