A PIECEWISE LINEAR APPROXIMATION FOR OUTPUT CHARACTERISTIC FOR SHORT-CHANNEL "EXTRINSIC" MOSFET WITH ACCOUNTING OF NONZERO DIFFERENTIAL CONDUCTANCE IN SATURATION REGIME AND SOURCE PARASITIC RESISTANCE EFFECT AT HIGH DRAIN BIASES

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Previously, we transformed the linear drain bias asymptote equation for the MOSFET drain current in the saturation regime from the "intrinsic" (without accounting for the contact and parasitic series resistances) case into "extrinsic" (with accounting for the contact and parasitic series resistances) case with accounting for the velocity saturation effect. As a result, we obtained the equation for the drain current that yielded the nonlinear dependence on the "extrinsic" drain bias for the short-channel "extrinsic" MOSFET in saturation regime in an implicit form. This equation can be solved numerically in the entire range of the "extrinsic" drain bias. Using this extrinsic equation, we derived the equation for the differential conductance of the "extrinsic" MOSFET at the "saturation point". Such "saturation point" is determined by the saturation current and saturation voltage equations for the "extrinsic" MOSFET that are well known from literature. We proposed a linear approximation for the dependence of the short-channel "extrinsic" MOSFET drain current on the "extrinsic" drain bias in the saturation regime. This approach works well for not very high drain bias.

In this paper, we analyze the previously obtained nonlinear equation for the short-channel "extrinsic" MOSFET drain current I_d and derive for one the asymptotic value V_{gt} / R_S for the "extrinsic" drain bias V_{ds} tending to infinity. Here V_{gt} is the "extrinsic" gate-to-source bias centered on threshold voltage and R_S is the source parasitic resistance. Note, that in this asymptotic case "intrinsic" centered gate-to-source bias ($V_{GT} = V_{gt} - I_d R_S$) tending to zero. Finally, we propose a piecewise linear approximation for the drain current dependence of a short-channel "extrinsic" MOSFET on the drain-to-source bias. This dependence includes the linear triode regime, the linear saturation regime and the regime with constant asymptotic drain current due to source parasitic resistance effect at high drain biases. We also suggest an approach for smoothing this piecewise linear approximation. These results can be applied for other types of field-effect transistors, like thin-film transistor (TFT) and organic field-effect transistor (OFET), as well. Thick solid line on Figure 1 - a piecewise linear approximation for short-channel "extrinsic" MOSFET drain current dependence on drain-to-source bias ($V_{gt} / V_L = 2$, $R_S \times \beta \times V_L = 5$, $R_D \times \beta \times V_L = 2$, $\alpha = 1.1$, $\lambda \times V_L = 1$). Here V_L - characteristic voltage, related to the drift velocity saturation in high electric field, β - MOSFET transconductance parameter, α - dimensionless saturation parameter, λ - channel-length modulation parameter, R_D - drain parasitic resistance. Thin solid lines – saturation current and saturation voltage levels. Dashed line – numerical solution of the equation for the drain current that yields the nonlinear dependence on the "extrinsic" drain bias for the short-channel "extrinsic" MOSFET in saturation regime. 2 dots 1 dash – exact solution without accounting for the velocity saturation effect. In this case we have cubic equation with respect to "intrinsic" centered gate bias V_{GT}. 2 dots 3 dashes - solution of quadratic equation obtained from cubic one with neglected cubic term, that is good approximation with V_{GT} tending to zero while V_{ds} tending to infinity.

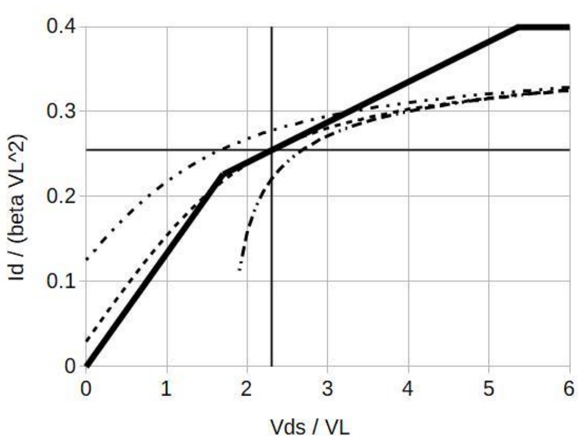

Figure 1 – A piecewise linear approximation for short-channel "extrinsic" MOSFET drain current dependence on drain-to-source bias